A Few Guidelines for SET Characterization of Non-Volatile FPGAs: Lessons Learned

Actel®
POWER MATTERS

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Outline

1. Motivations & Objectives
2. Non-Volatile FPGAs
   1. **Antifuse-Based FPGAs (RTAX-S)**
   2. **Flash-Based FPGAs (ProASIC3) => New RTA3PL**
3. Lessons Learnt
   1. **SET Sensitivities: FPGA Technology & Architecture**
   2. **SET Propagation: Timing Constraints**
4. Summary

Motivations

Non-Volatile Under Radiation

- **FPGA Configuration Memory can not UPSET**
  - **FPGA Switches are NOT Memory Bits**
  - **Antifuse: Hard Switches (Metal to Metal)**
  - **Flash: FG Transistors ('ON' or 'OFF' and NOT '0' and '1)**
- **Single-Chip Solution => Higher Reliability and Lower-Power**

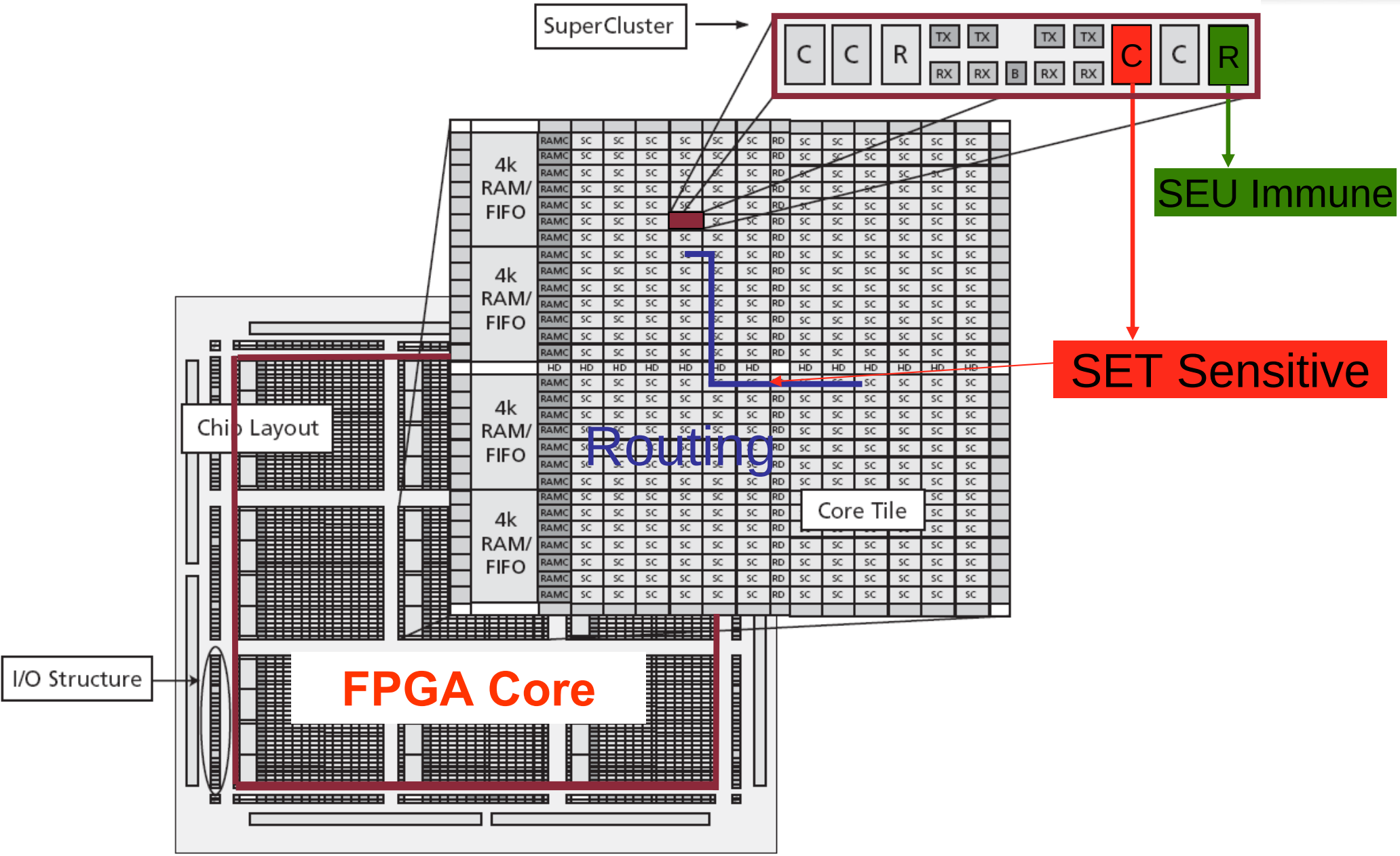
Radiation SEE Sensitivities

- **SET Effects could be isolated from SEU Effects**
  - **Sequential Logic (SEU) & Combinatorial Logic (SET)**
- **SEU Immunity by TMR & SET Immunity by SET filtering**

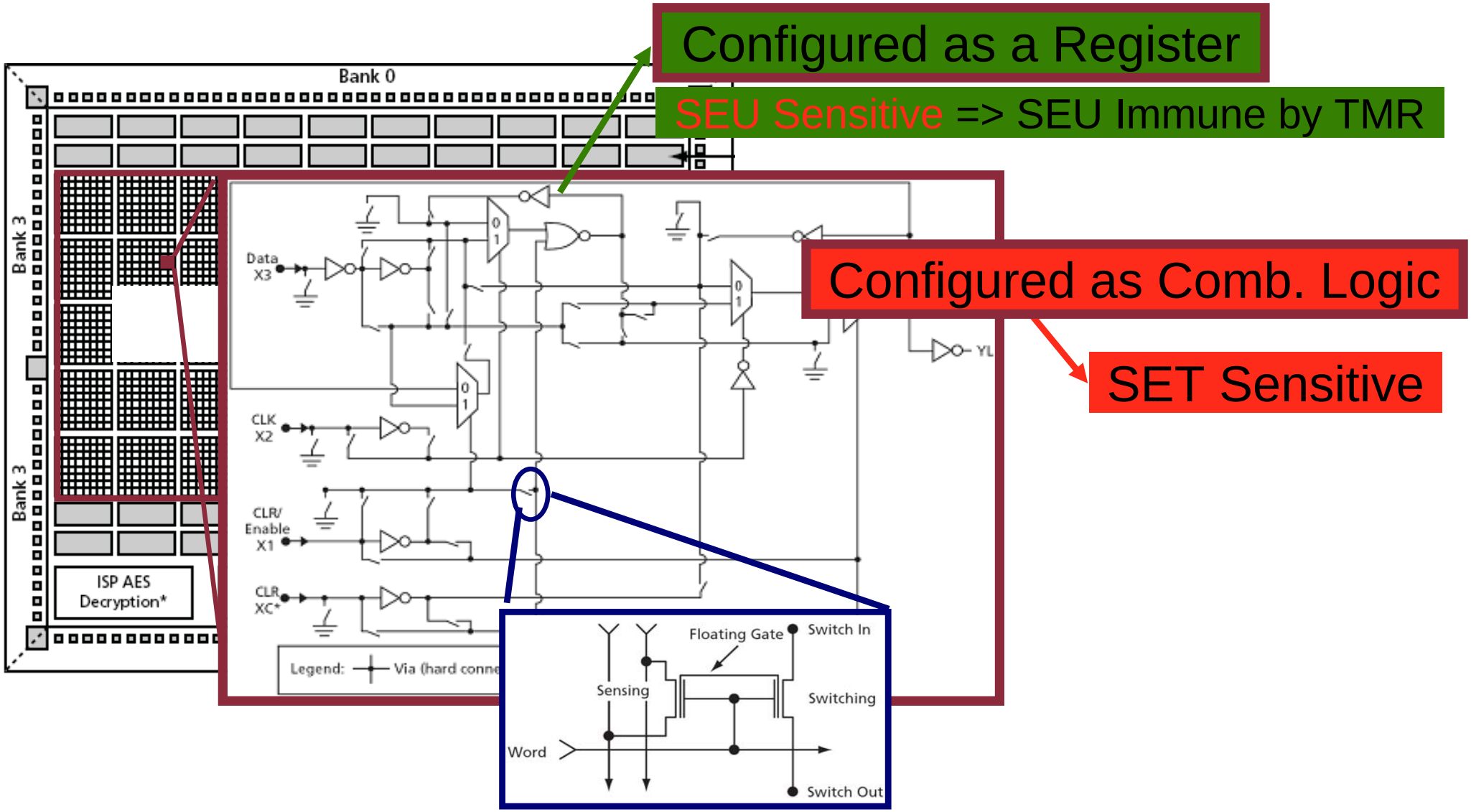
Lessons Learnt

- **SET Sensitivities: FPGA Technology & Architecture, etc.**
- **SET Propagation: Timing Constraints, etc.**

RTAX-S FPGA Features (0.15 µm)



ProASIC3 FPGA Features (0.13 um)



SET in Non-Volatile FPGAs

- SET Cross-Sections
  - **FPGA Technology & Architecture**
  - **FPGA Configuration (Test Design)**
  - **Test Design's Frequency**

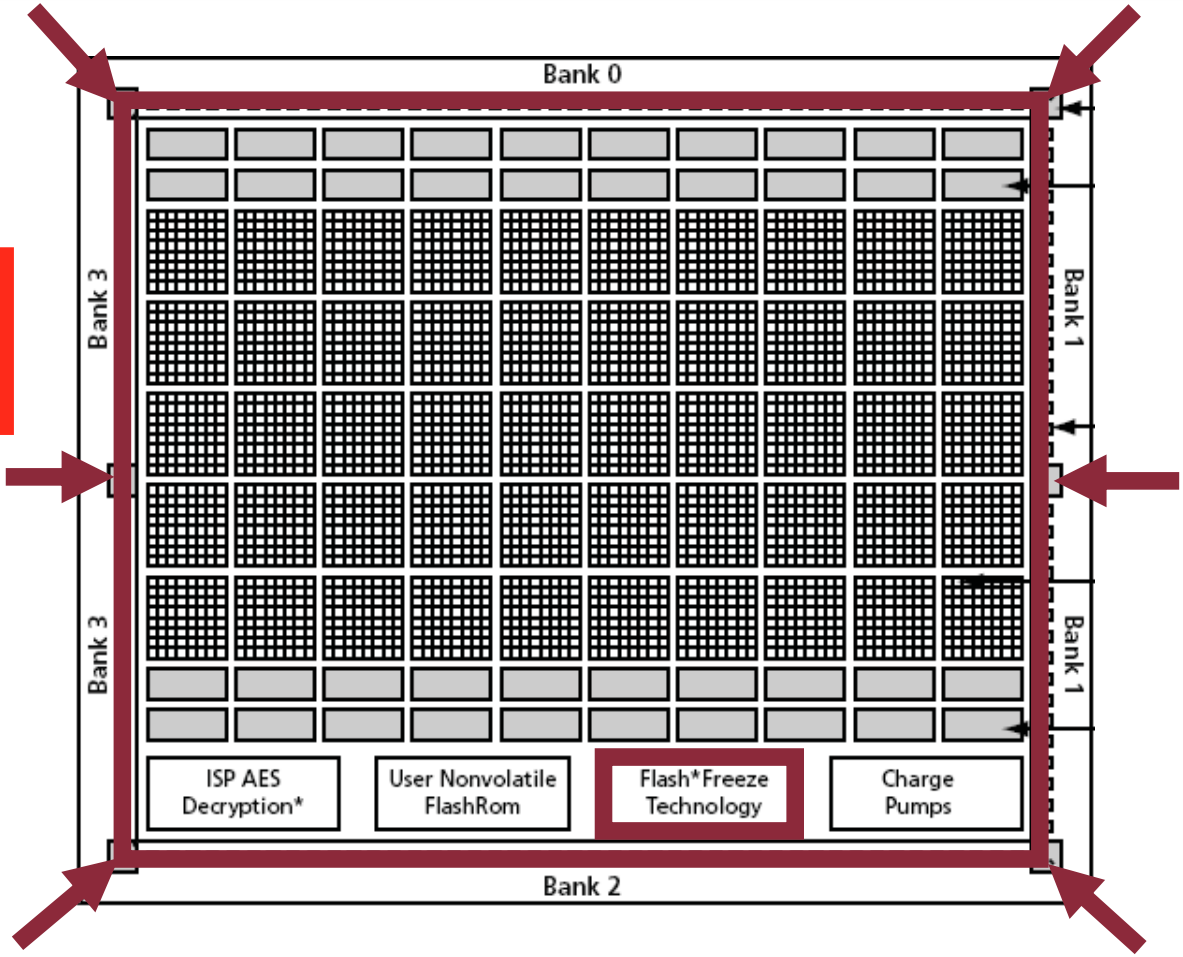
1. SET First Hit (Pulse Shape & Width)
   - **FPGA Technology**
   - **Minimum Setup Time of a Logic Cell (Inverter)**
2. SET Propagation
   - **FPGA Technology & Architecture**
   - **Test Design Configuration & Connectivity**

SET Guidelines and Lessons Learnt

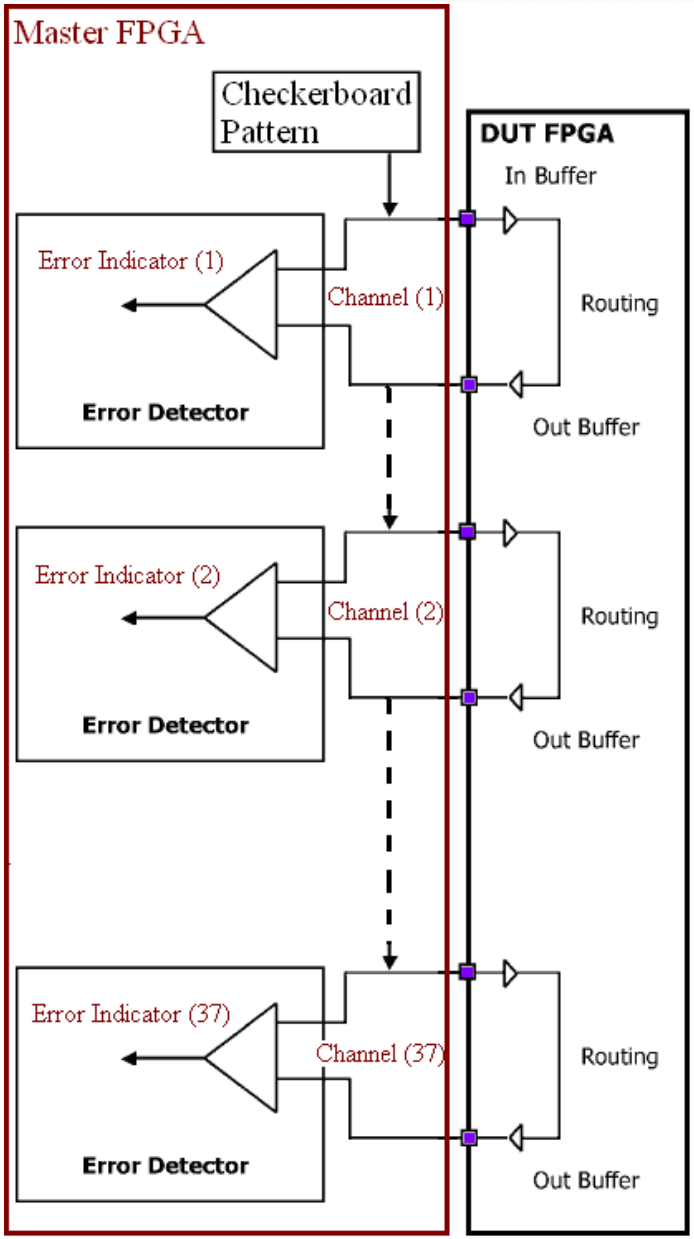
- **G1: FPGA's Global Signals (Global Errors)**
- **G2: FPGA Technology, Architecture & Size**
- **G3: FPGA Design's Configuration & Connectivity**
- **G4: FPGA's Design's Timing Constraints**

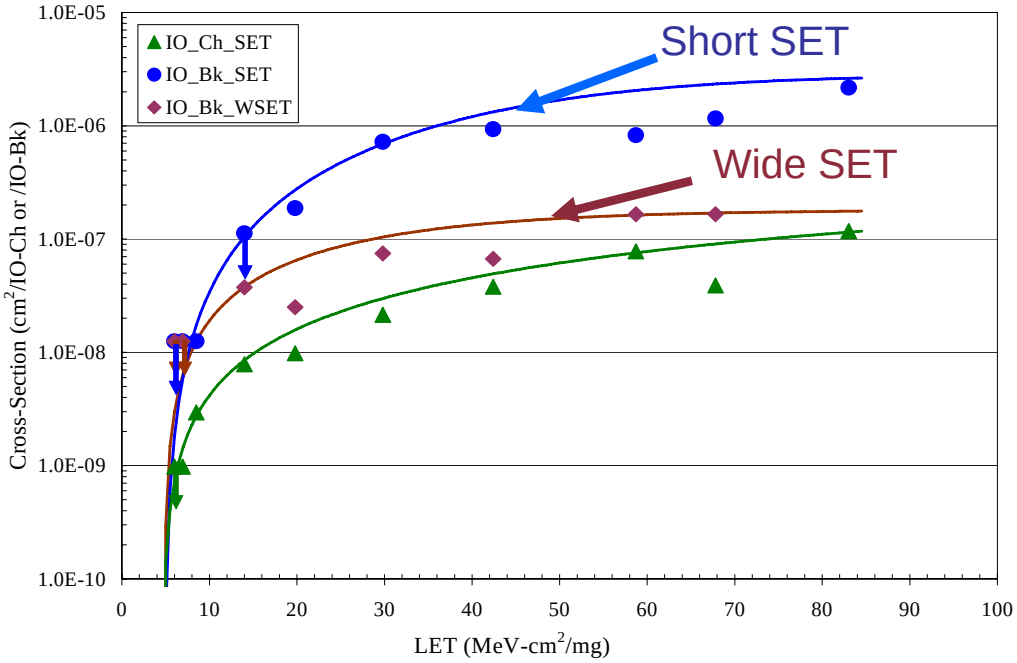
Guideline 1: Global Signals

- Power-Up Signals (Flash-Freeze)
- Enable of an IO Bank or the entire DUT IOs
- Global Clock and Reset Signals
- Etc.



Example 1: IO Test Design

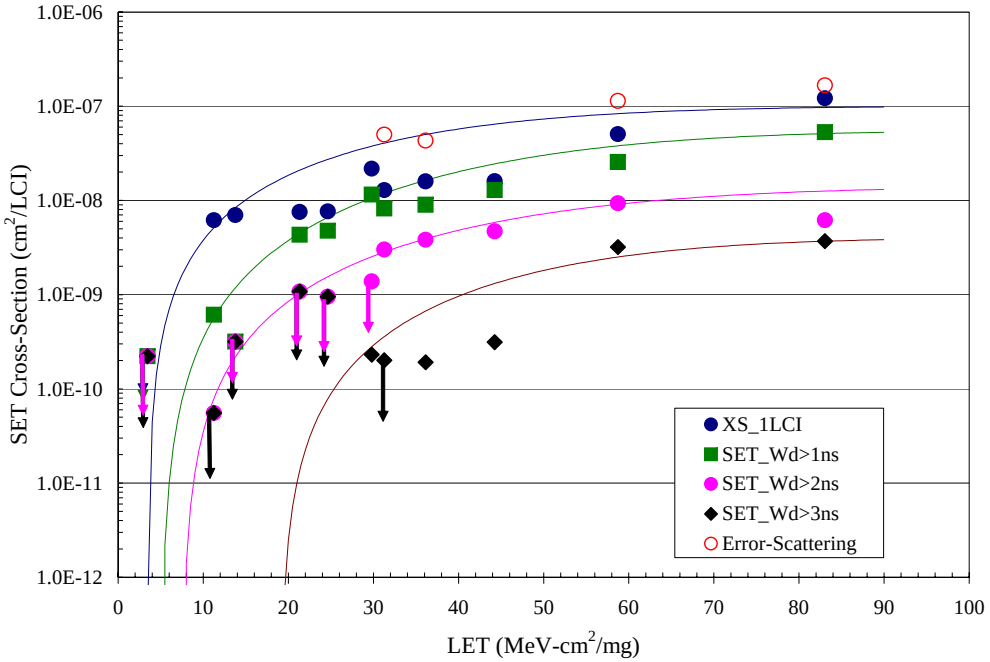




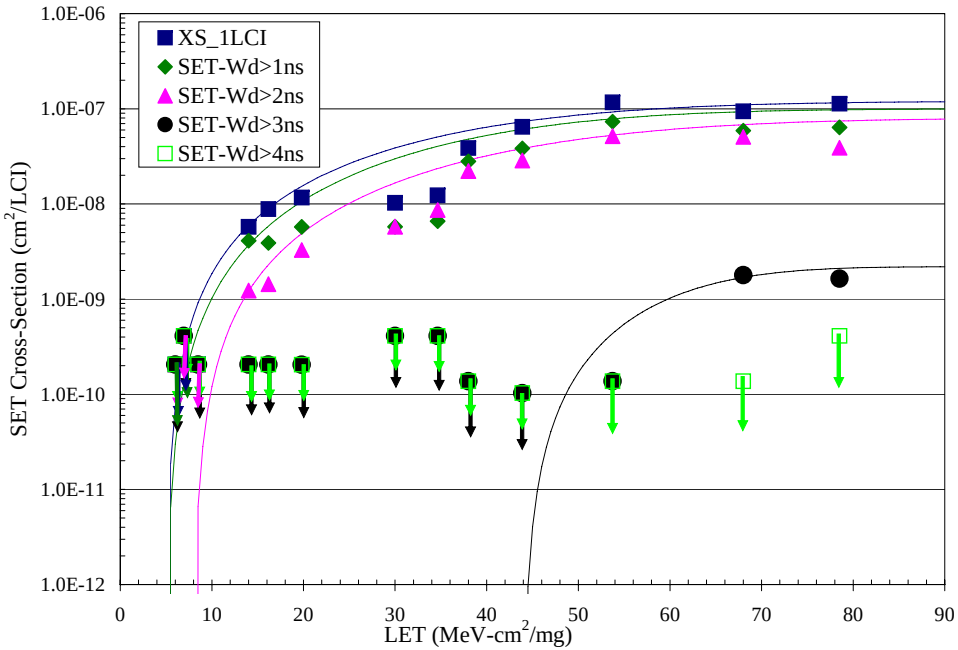
- SET on single IO channels
- SET on the global enable signal of a single IO bank, observed mostly at 50 MHz
  - Short SET < 40 ns, XS = 2×10^{-6} cm²/IO-Bk
  - **Wide SET < 250 ns , XS = 1.7×10^{-7} cm²/IO-Bk**

Example 1: IO Test Design (Cont'd)

1. Without IO Bank Mitigation



2. With IO Bank Mitigation



Reminder: Global Signals must be tested at High Frequencies to measure their maximum SET Pulse width

G2: Technology, Architecture & Size

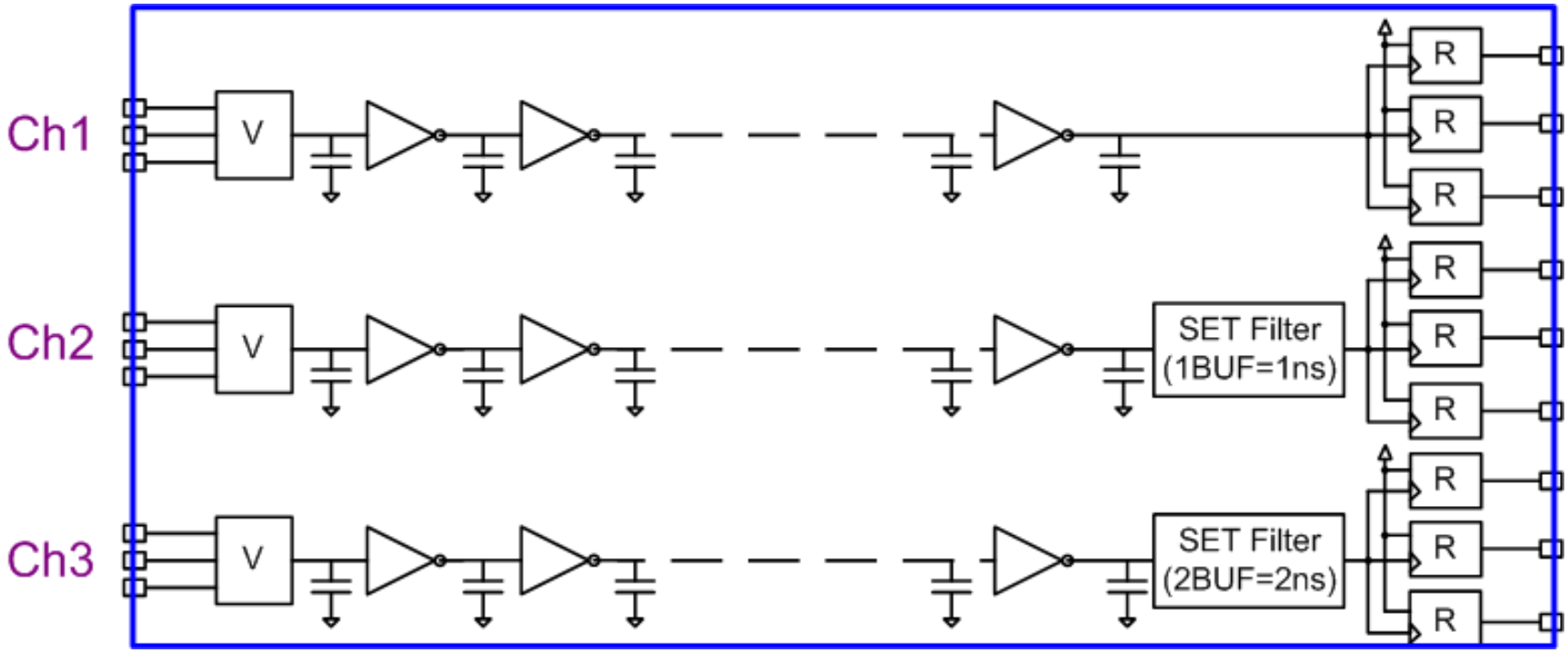
Device Technology & DUT Size

- **DUT Density and Geometry**
- **Studied Cases:**
  - **Antifuse-FPGA: RTAX250S, RTAX2000S (0.15 µm)**
  - **Flash-FPGA: A3P250 (0.13 µm)**

FPGA Architecture

- **SET Sensitivity of the FPGA Switches (A3P but Not RTAX)**
- **Logic Cell Architecture**
  - **Strictly Combinatorial (RTAX)**
  - **Combinatorial & Sequential (A3P)**

Example 2: SET Characterization

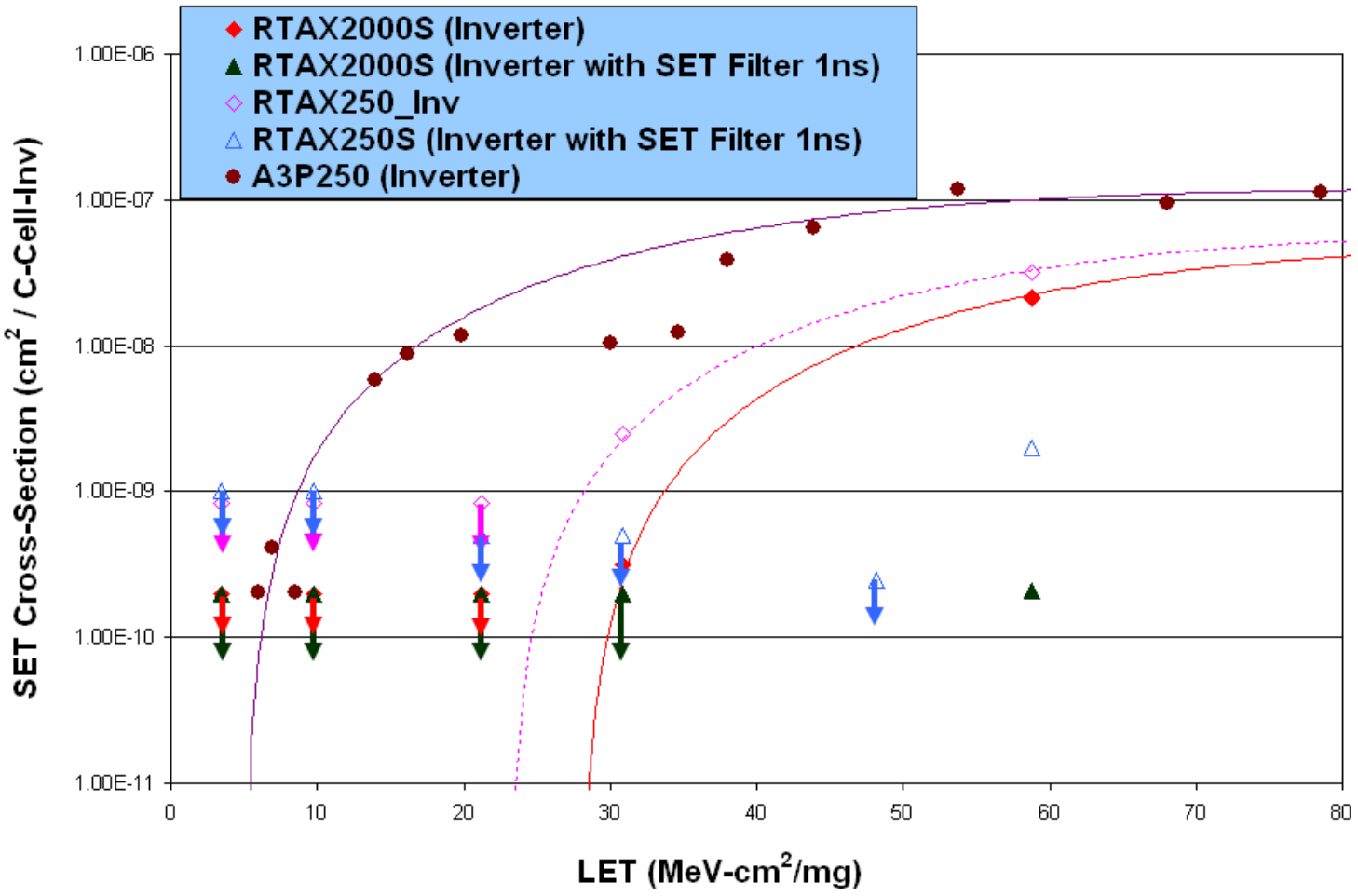


Design / FPGA	# Inverters / Channel
RTAX250S	120
RTAX2000S	950
A3P250	486

Example 2: SET Characterization (Cont'd)

SET Cross-Sections and Pulse Widths

- **FPGA Technology and Architecture**
- **FPGA Densities and Geometries**



G3: Configuration & Connectivity

1. Device Under Test: RTAX250S

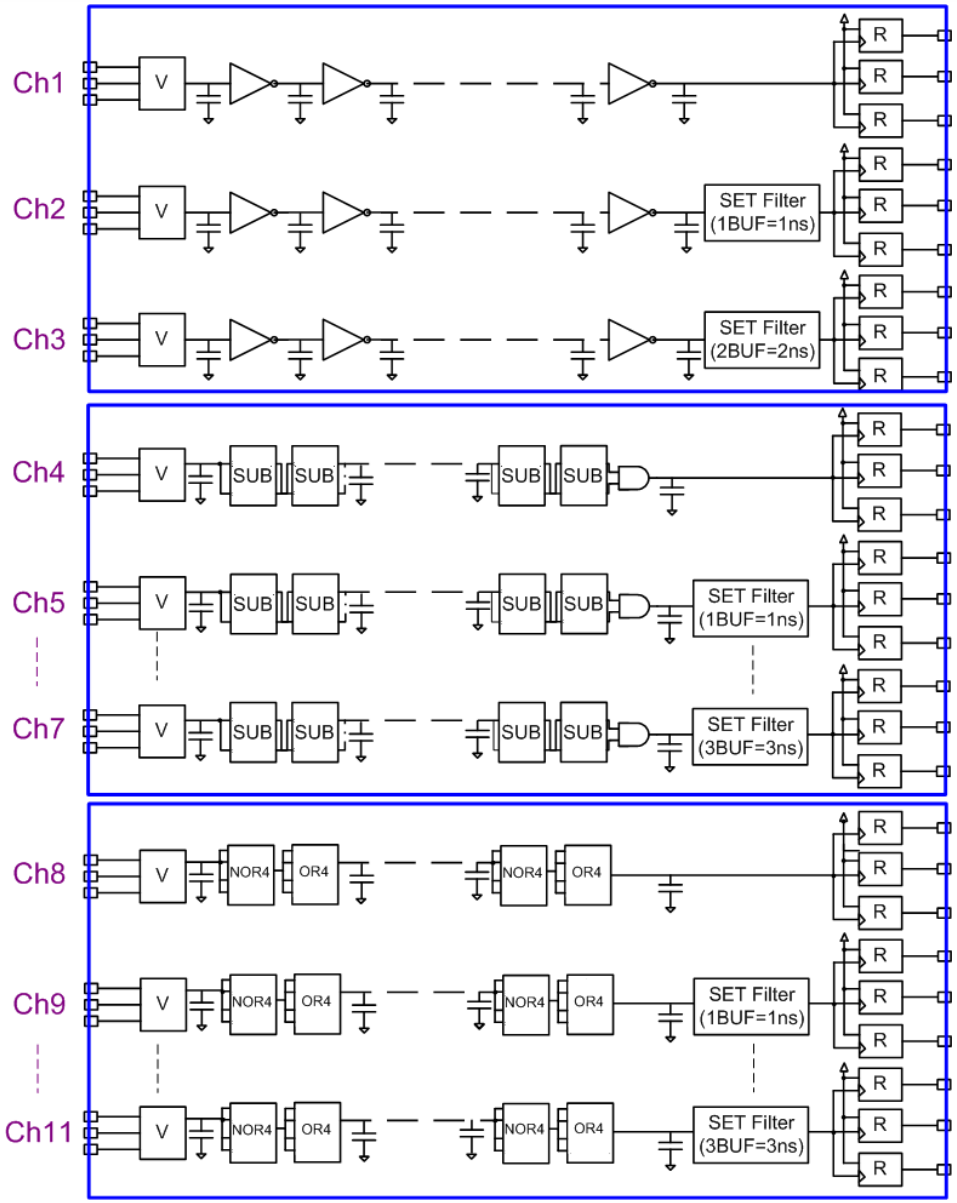
2. FPGA Configuration & Connectivity

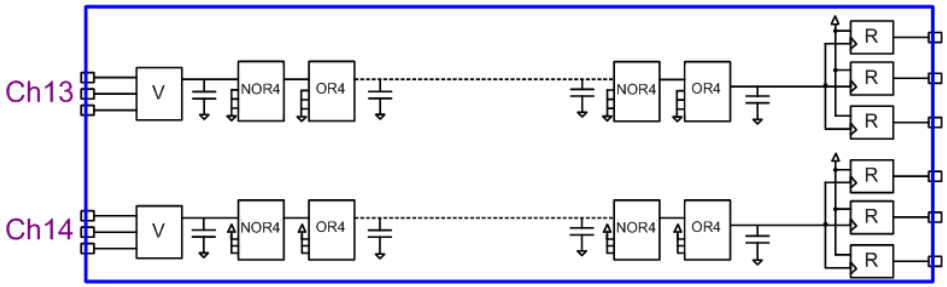
- **Minimum Logic Cell Area (Inverter)**
- **Carry-Chain (Subtractor: SUB1)**
- **Maximum Logic Cell Area (OR4 Gate)**
  - **3 Inputs of the OR4 Gate are grounded**
  - **3 Inputs of the OR4 Gate are biased high**
  - **All 4 inputs of the OR4 Gate are tied together (Unrealistic Case: automatically trimmed by the Vendor Software Tools)**

3. SET Characterization

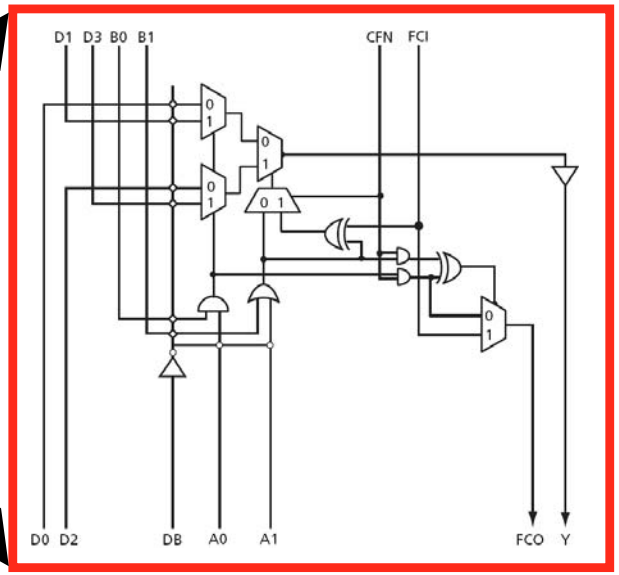
1. **SET Cross-Section per Logic Cell**
2. **Maximum SET Pulse-Width for a given Logic Cell**

Example 3: SET Characterization





RTAX C-Cell



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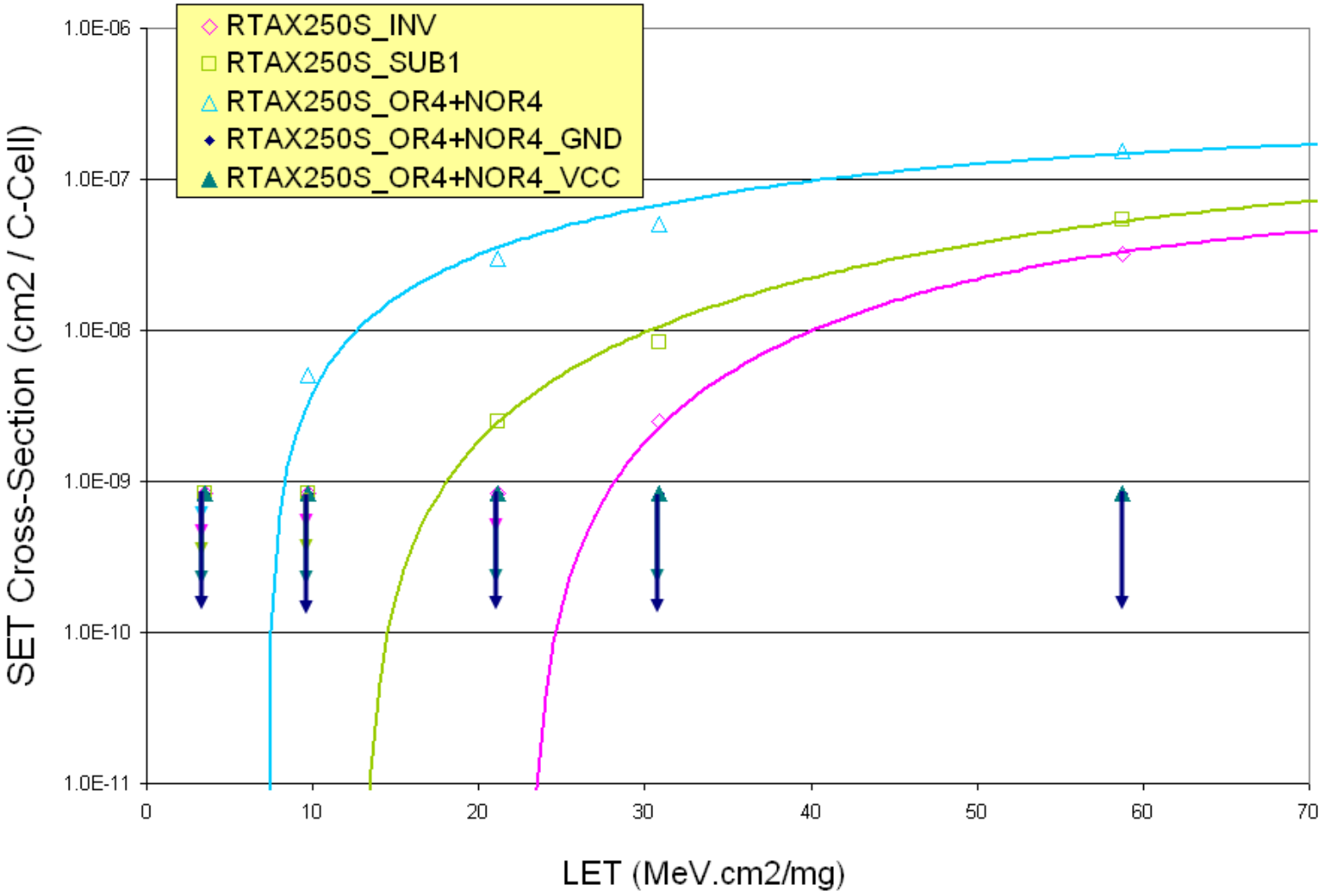
RTAX2000S	950

Example 3: SET Characterization (Cont'd)

- Very Little SET Sensitivity for Real Designs in the RTAX-S



G3: Configuration & Connectivity (Cont'd)

Test Design Configuration

- **Worst-Case Time-Configuration (Min. Setup-Time (Inverter))**
- **Worst-Case Area-Configuration (Max. Logic Cell Area (OR4 Gates))**

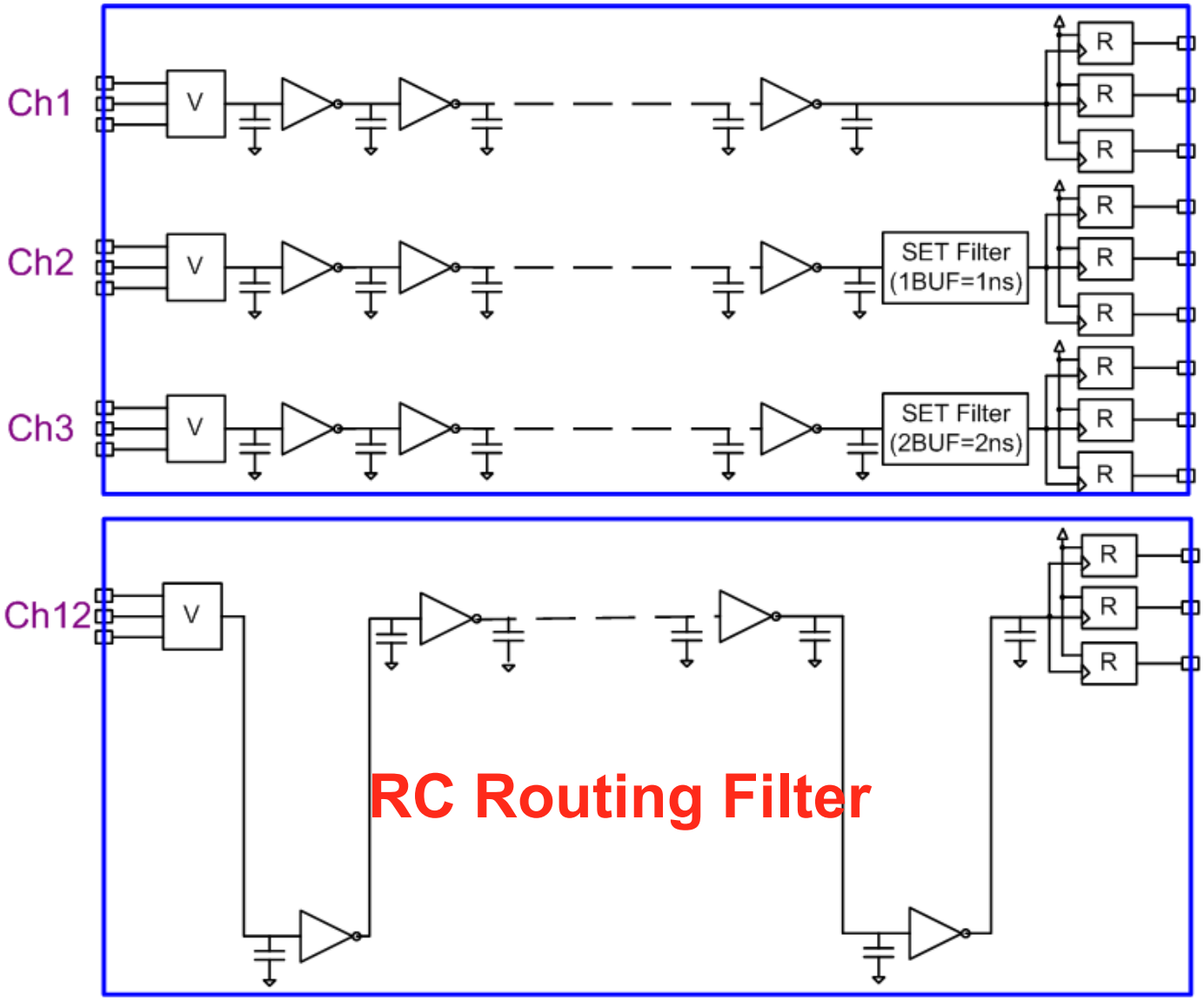
Test Design Connectivity

- **Real Test Designs (Not trimmed by the Vendor Software)**
- **Use Worst-Case Design's Connectivity**

Guideline 4: SET Propagation

- DUT
  - **RTAX250S and RTAX2000S**
  - **ProASIC3 (NSREC 2008)**
- SET Pulse Transition (Positive & Negative)
  - **See NSREC 2008 Rezgui et al. Paper, TNS 08**
- Spontaneous SET RC Filter in Non-Volatile Circuits
  - **Various Routing**

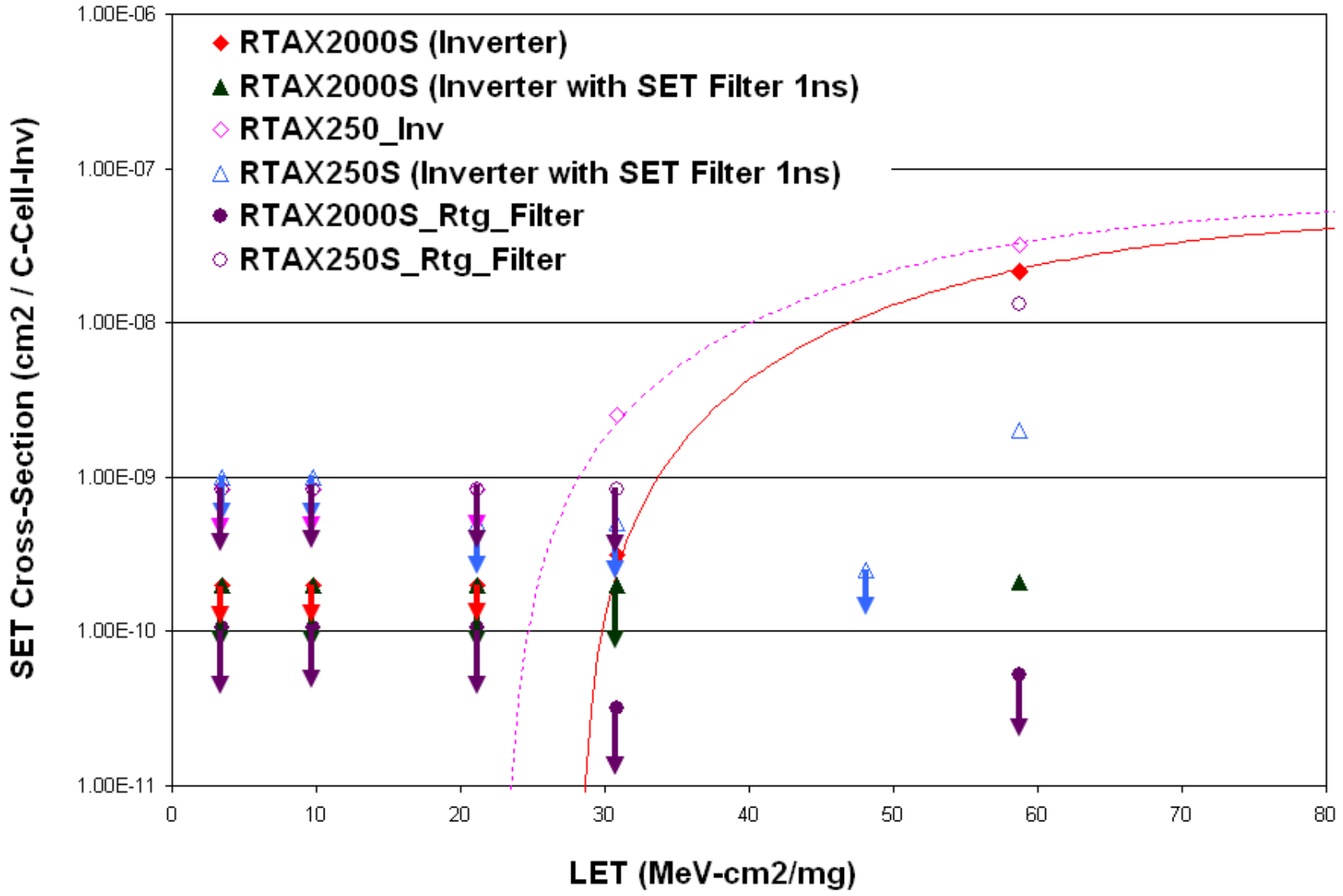
Example 4: SET Propagation



Design / FPGA	# Inv / Ch
RTAX250S	120
RTAX2000S	950

Example 4: SET Characterization (Cont'd)

Spontaneous SET Filtering in the RTAX FPGA



Summary & Lessons Learnt

1. Checklist for SET Characterization

1. **Is the FPGA Configuration Memory Non-Volatile Under Radiation?**
2. **What are the FPGA's Global Signals?**
3. **What are the Worst-Case Logic Cells Configuration & Connectivity?**
4. **How do SET Propagate in the FPGA (Architecture, Technology, SET Pulse Polarity, etc.)?**

2. Good SET Characterization

1. **Full SET immunity after mitigation of all SET you think you have found….**
2. **Use Real Test Designs (equal probabilities of negative and positive transitions)**
3. **Timing Simulation & Fault Injection are Mandatory prior to Radiation Test Experiments.**